ABSTRACT

A copy protection system for a field programmable gate array includes a factory-programmed logic device (CPLD) including an initial state generator, a first sequence generator and an encryption device and a field-programmable gate array device (FPGA) being programmed with a field-programmable gate array program and including a second sequence generator, a third sequence generator, a decryption device and a sequence comparison device, the second sequence generator being a replicate of the first sequence generator. The CPLD generates an initial state in the initial state generator, initializes the first sequence generator with the initial state, encrypts the initial state in the encryption device, and transmits the encrypted initial state to the FPGA. The FPGA decrypts the encrypted initial state in the decryption device, initializes the second sequence generator with the initial state, generates a challenge sequence with the third sequence generator, transmits the challenge sequence to the first sequence generator and the second sequence generator. The first sequence generator generates a first reply sequence based on the initial state and the challenge sequence and transmits the first reply sequence to the sequence comparison device, and the second sequence generator generates a second reply sequence based on the initial state and the challenge sequence and transmits the second reply sequence to the sequence comparison device, which compares the first and second reply sequences and enables operation of the FPGA program when the first and second reply sequences are identical.